SREENIVASA INSTITUTE OF TECHNOLOGY AND MANAGEMENT STUDIES

(Autonomous)

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

QUESTION BANK

20ECE 237 – SWITCHING THEORY AND LOGIC DESIGN

Question No.	Questions	PO Attainment
	UNIT – I	
	PART A (2 Marks)	
1	What you mean by weighted code?	PO1
2	Discuss octal number system.	PO1
3	111001-1010 Subtraction by using 2's complement.	PO1
4	Define Associate Law and Distributive Law of Boolean functions.	PO1
5	Convert $(1341)_{10} = (\ )_{16}$	PO1
6	State about error correcting codes?	PO1
7	Explain the importance of gray code	PO1
8	Design EX-OR gate using NAND gates only	PO1
9	Convert $(225.225)_2$ to octal	PO1
10	Define Boolean Algebra.	PO1
11	Discuss 1"s and 2"s complement methods of subtraction.	PO1
12	What are the universal gates? Why they are called universal gate?	PO1
13	Differentiate between binary code and BCD code?	PO1
14	List the steps to obtain dual of a given Boolean Expression.	PO1
15	Draw the truth table of NOR gate.	PO1
	PART-B (10 Marks)	
1	Perform the subtraction with the following binary numbers by taking the 2's complement of the subtrahend: (i) 100 – 110000 (ii) 11010 - 1101.	PO1, PO2
2	a) Write short notes on binary number systems. b) Explain non-weighted codes	PO1, PO2
3	Perform arithmetic operation indicated below. (i).001110 + 110010 (ii). 101011 – 100110 iii)10110110/101	PO1, PO2
4	a)Explain 4-bit Gray-code and illustrate with examples and also give its applications. b)convert $(FACE)_{16}$ into its equivalent octal number	PO1, PO2
5	a) Explain about error detection codes. b) What is Hamming code? Generate Even parity Hamming code for a given binary data 1101	PO1, PO2
6	(a)Convert the following numbers i. $(4567)_{10}$ to base 8. ii. $(53.1575)_{10}$ to base 2. iii. $(456)_{10}$ to BCD equivalent. (b) What are the Universal gates? Why they call as Universal gates?	PO1, PO2
7	(a)Convert the following numbers $(786)_{10}$ to BCD,excess -3 equivalent. (b) Draw the logic circuit for the following Boolean expression.	PO1, PO2

	f = AC+ABC($\bar{A}$ B +AC) f = AC+ABC($\bar{A}$ B +AC)	
8	(a)Simplify to a sum of 3 terms: A'C'D' +AC' +BCD + A'CD' + A'BC +AB'C' (b) Simplify F=ABC+AB'C+ABC'	PO1, PO2
9	Express the function in SOP and POS. i) (AB+C) (B+C'D) ii) X'+X (X+Y') (Y+Z')	PO1, PO2
10	(a) Simplify the following Boolean functions to a minimum number of literals a) X +X'Y b) XY + X'Z + YZ (b) Find the complement of the functions F1 = X'YZ' + X'Y'Z by applying Demorgan's theorem.	PO1, PO2
11	(a) Express the function F=A+B'C in sum of products form (b) Express the function F=(A+B)(B+C) in product of sums	PO1, PO2
12	Implement EX-OR and EX_NOR gates using NAND gates only	PO1, PO2
13	Implement the given Boolean functions using basic gates i)F=(x+y)(y+z)' ii)F=xy+x'y'+y	PO1, PO2
14	(a)Encode the binary word $(1010)_2$ into seven bit even parity Hamming code. (b) The Hamming code $(101101101)_2$ is received. Correct it if any errors, there are four parity bits & odd parity is used.	PO1, PO2
15	(a) Subtract $(111001)_2$ from $(101011)_2$ using 1's complement. (b) Subtract $(101011)_2$ from $(111001)_2$ using 2's complement.	PO1, PO2

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Question No.	Questions	PO Attainment
	UNIT – II	
	PART A (2 Marks)	
1	Explain 4 variable Karnaugh map.	PO1
2	Simplify the Boolean function x′yz + x′yz′ + xy′z′ + xy′z using K-map	PO1
3	Locate the minterms in a three variable k-map for f=Σm(0,1,5,7)	PO1
4	Minimize the Boolean expression $x + x'y$ using k-map	PO1
5	Minimize the Boolean function f (a, b, c) =∑ (2,3,5,7)	PO1
6	Define Don't Care Condition	PO1
7	Simplify the Boolean function f(x,y,z)=Σ(3,4,6,7)	PO1
8	Explain minterms	PO1
9	Explain maxterms	PO1
10	Express the Boolean function F(a,b,c)=ab+a'bc in a POS form	PO1
11	Minimize the function f (a, b, c) =∑ (0,3,5,7)	PO1
12	Simplify the Boolean expressions, ABC+A'B+ABC' to minimum no. of literals	PO1
13	Simplify the Boolean function x′yz + x′yz′ + xy′z′ + xy′z using K-map	PO1
14	Express the Boolean function F = A + B´C in a sum of minterms	PO1
15	Reduce the following expression using Karnaugh map ($B^1A + A^1B + AB^1$)	PO1
	PART-B (10 Marks)	
1	Simplify the following Boolean functions, using four-variable maps: a) F(w, x, y, z) = ∑ m(1, 4, 5, 6, 12, 14, 15) (5 marks) b) F(A, B, C, D) = ∑ m(0, 1, 2, 4, 5, 7, 11, 15) (5 marks)	PO1, PO2
2	Simplify the following Boolean functions, using four-variable maps: (a) F(A, B, C, D) = ∑ m(0, 1, 4,8,9,10) (5 marks) (b) F(A, B, C, D) = ∑ m(0, 1, 3, 4, 5, 7, 10, 13,14,15) (5 marks)	PO1, PO2
3	Simplify the following Boolean expressions using K-map and implement them using NOR gates: (a)F (A, B, C, D) = $AB^1C^1 + AC + A^1CD^1$ (b)F (W, X, Y, Z) = $W^1X^1Y^1Z^1 + WXY^1Z^1 + W^1X^1YZ + WXYZ$.	PO1, PO2
4	Simplify the following Boolean functions, using four-variable maps: (a) F(A, B, C, D) = ∑m(0, 3, 5, 6, 9,10, 12, 15) (5 marks) (b) F(A, B, C, D) = ∑m(0, 2, 4, 5, 6, 7, 8, 10, 13, 15) (5 marks)	PO1, PO2
5	Simplify the following Boolean functions, using four-variable maps: (a) F(A, B, C, D) = ∑m(0, 1, 2, 3,4, 6, 7, 8, 9, 11, 15) (5 marks) (b) F(A, B, C, D) = ∑m(0, 2, 3, 5, 7, 8,10,11,14, 15) (5 marks)	PO1, PO2
6	Simplify the following Boolean functions, using four-variable maps: (a) F(A, B, C, D) = ∑m(5, 6,7, 12, 13) +d(4,9,14,15) (5 marks) (b) F(A, B, C, D) = ∑m(1, 3, 5, 8, 9,11, 15) +d(2,5) (5 marks)	PO1, PO2

7	Simplify the following Boolean functions, using four-variable maps: (a) F(A, B, C, D) = ∑m(1, 4, 8, 9, 13,14, 15)+d(2,3,11,12) (5 marks) (b) F(A,B,C,D)=ΠM(0,2,3,8,9,12,13,15)	PO1, PO2
8	Simplify the following Boolean functions, using five-variable maps: F(A, B, C, D) = ∑ m(1, 3, 5, 9, 11, 15)+d(2,13) (5 marks) F(A, B, C, D,E) = ∑m(0, 1, 4, 5, 16, 17, 21, 25, 29) (5 marks)	PO1, PO2
9	Simplify the Boolean function using K-Map a) F(A,B,C,D,E)= ∑m(0,1,4,5,7,11,15,28,29,30,31) b)F(A,B,C,D)= ∑m(1,3,7,11,15)+ ∑ d(0,2,4)	PO1, PO2
10	Simplify the following Boolean functions, using five-variable maps: F(A, B, C, D,E) = ∑m(0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31) F(A, B, C, D) = ∑ m(0, 1, 4, 5,6, 7, 9,11, 15) +d(10,14) (5 marks)	PO1, PO2
11	Simplify the following Boolean functions, using five-variable maps: F(A, B, C, D,E) = ∑m(0, 5, 6, 8, 9, 10, 11, 16, 20, 24, 25, 26, 27, 29, 31)	PO1, PO2
12	Simplify the following Boolean functions, using five-variable maps: F(A, B, C, D,E) = ∑ m(1, 4, 8, 10, 11, 20, 22, 24, 25, 26) +d(0,12,16,17)	PO1, PO2
13	Simplify the following Boolean functions, using five-variable maps: F(A, B, C, D,E) = ∑ m(0, 1, 4, 5, 6, 10, 14, 16,20,21,22,26,30)	PO1, PO2
14	Simplify the Boolean function F=A'B'C'+B'CD'+A'BCD'+AB'C' using K-map	PO1, PO2
15	Simplify the Boolean function F=1,3,4,5,6,12,24,26,28,31,36,37,36,38,39,40,42,44,50,53,53,55,60 using K-Map	PO1, PO2

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Question No.	Questions	PO Attainment
	UNIT – III	
	PART A (2 Marks)	
1	Define magnitude comparator?	PO1
2	Implement 4:1 multiplexer	PO1
3	List the procedural steps to add two BCD numbers	PO1
4	Describe the differences between PLA and PAL	PO1
5	Give the expression for Borrow and Difference in a Full Subractor.	PO1
6	Give the expression for Sum and Carry in a Half Subractor.	PO1
7	List the Drawbacks of PLA	PO1
8	Define combinational circuit	PO1
9	Draw the truth table and logic diagram of decoder	PO1
10	Draw the logic diagram of Half Adder	PO1
11	Write the truth table of Full Adder	PO1
12	Define Multiplexer	PO1
13	Give the applications of Multiplexer.	PO1
14	Define De-Multiplexer	PO1
15	Draw PLA architecture	PO1
	PART-B (10 Marks)	
1	Design Full adder by using half adders and draw truth table	PO1, PO2,PO3
2	Design half subtractor and full subtractor using logic gates	PO1, PO2,PO3
3	Explain And Design 3:8 decoder and draw the logic diagram	PO1, PO2,PO3
4	Explain and Design how a Carry look ahead adder speeds up the addition process.	PO1, PO2
5	A combinational circuits is defined by the function F1(A, B, C) = Σ(3, 5, 6, 7), F2(A, B, C) = Σ(0, 2, 4, 7) implement the circuits with a PLA having 3 inputs 4 Product terms and 2 outputs.	PO1, PO2,PO3
6	Design two bit magnitude comparator with logic gates	PO1, PO2,PO3
7	Implement with PAL. W (A,B,C,D) = Σ (2,12,13) X (A,B,C,D) = Σ (7,8,9,10,11,12,13,14,15) Y(A,B,C,D) = Σ (0,2,3,4,5,6,7,8,10,11,15) Z (A, B,C,D) = Σ (1,2,8,12,13)	PO1, PO2,PO3

8	Explain BCD adder with example and draw block diagram	PO1, PO2,PO3
9	Design 2X4 decoder and implement 3X8 decoder	PO1, PO2,PO3
10	a) Implement the following Boolean function using PLA F (W,X,Y,Z)=(0,1,3,5,9,13) b) Compare all programmable logic devices	PO1, PO2,PO3
11	Design Full adder and Full subtractor using 3X8 Decoder	PO1, PO2,PO3
12	Design and Explain Decimal to BCD Encoder	PO1, PO2,PO3
13	a)Design 1X8 DEMUX using 1X4 DEMUXEs b)Implement Full subtractor using demultiplexer	PO1, PO2,PO3
14	Design a combinational circuit using a PROM, which accepts 3 bit binary number and generates its equivalent Excess-3 code	PO1, PO2,PO3
15	Design 32X1 MUX using four 8X1 MUX and 2X4 Decoder	PO1, PO2,PO3

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Question No.	Questions	PO Attainment
	UNIT – IV	
	PART A (2 Marks)	
1	What is a Flip-Flop?	PO1
2	What are the applications of Flip-Flops?	PO1
3	What is the difference between Synchronous and asynchronous sequential circuits?	PO1
4	Write the excitation table of a RS and D-FFs	PO1
5	Give the truth table of D-flip-flop with symbol	PO1
6	Draw the logical diagram of serial-in and parallel-out shift register.	PO1
7	Explain about T flip flop.	PO1
8	Why a gated D latch is called a transparent latch?	PO1
9	Show the logic diagram of SR flip-flop with NAND gates	PO1
10	what are the differences of flip-flop and Latch?	PO1
11	Differentiate between combinational and sequential circuits	PO1
12	What is race around condition?	PO1
13	What are Shift registers?	PO1
14	Discuss about a bidirectional shift register?	PO1
15	What are the applications of shift registers?	PO1
	PART-B (10 Marks)	
1	Explain about all flip flops in detail with diagram	PO1, PO2
2	Design BCD counter using JK flip-flop	PO1, PO2
3	Draw and explain 4 bit Johnson counter. Draw the timing diagram also.	PO1, PO2
4	Describe about T – Flip-flop with the help of a logic diagram and characteristic table. Derive a T-flip-flop from JK and D flip-flops.	PO1, PO2
5	Explain the operation of SR Flip-Flop using asynchronous inputs with truth table.	PO1, PO2
6	Convert a JK FF to i) SR ii) T iii) D	PO1, PO2
7	Design a decade counter and explain its operation.	PO1, PO2,PO3
8	Give the transition table for the following flip-flops i) SR FF ii) D FF	PO1, PO2
9	Design a mod 6 asynchronous up counter using T flip-flop	PO1, PO2,PO3
10	Design a Modulo-12 up Synchronous counter Using T-Flip Flops and draw the Circuit diagram	PO1, PO2,PO3
11	Draw and explain i) serial in serial out shift register ii) serial in parallel out shift register	PO1, PO2,PO3
12	Draw and explain i) parallel in serial out shift register ii) parallel in parallel out shift register	PO1, PO2,PO3

13	a) Draw and explain bidirectional shift register b)Compare synchronous and asynchronous counters	PO1, PO2,PO3
14	Draw and explain universal shift register	PO1, PO2,PO3
15	Draw and explain master slave JK flip-flop and also draw timing diagrams	PO1, PO2,PO3

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Question No.	Questions	PO Attainment
	UNIT – V	
	PART A (2 Marks)	
1	What are the capabilities of FSM?	PO1
2	What is characteristic table and excitation table?	PO1
3	List the advantage of having equivalent states?	PO1
4	State equivalence theorem	PO1
5	Define mealy machine with block diagram	PO1
6	List the steps in reduction of state tables.	PO1
7	Define Moore machine	PO1
8	What is state assignment	PO1
9	What is meant by ASM chart	PO1
10	Draw the symbols of ASM Building Blocks	PO1
11	Define State diagram	PO1
12	Define State table	PO1
13	Differentiate Mealy and Moore State Machines.	PO1
14	What is the difference between Flow chart and ASM chart?	PO1
15	Draw the ASM Chart for D-Flip Flop	PO1
	PART-B (10 Marks)	
1	Explain the state reduction and state assignment in designing sequential circuit. Consider one example in this process	PO1, PO2
2	a) List the capabilities and limitations of Finite state machines b)Write design procedure for clocked sequential circuits	PO1, PO2
3	Write the differences between Mealy and Moore type machines.	PO1, PO2
4	Explain the concept of ASM chart? And also give the brief description of ASM Components	PO1, PO2
5	Draw the ASM chart for SR Flip-Flop & JK Flip-Flop.	PO1, PO2, PO3,PO4
6	Design a sequence detector which detects 10101 using T flip-flops.	PO1, PO2,PO3
7	Draw the block diagram of Moore and mealy circuits and give a comparison table of these circuits.	PO1, PO2, PO3,PO4
8	With suitable example explain a) State table b) State diagram c) State equivalence.	PO1, PO2
9	Draw an ASM chart for a 2-bit binary counter having one enable line E such that: E=1(counting enabled) E=0(counting disabled)	PO1, PO2, PO3,PO4
10	Draw ASM chart for serial adder	PO1, PO2, PO3,PO4

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<td>11</td>
<td>Design a clocked sequential circuit for the given state table
Using D-flip flop
<table>
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<tr><td>X=0</td><td>X=1</td></tr>
<tr><td>A</td><td>F,0</td><td>B,1</td></tr>
<tr><td>B</td><td>G,0</td><td>A,1</td></tr>
<tr><td>C</td><td>B,0</td><td>C,1</td></tr>
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<tr>
<td>12</td>
<td>Design a clocked sequential circuit for the given state table
Using JK flip flop
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<tr><td>A</td><td>A,0</td><td>B,0</td></tr>
<tr><td>B</td><td>C,0</td><td>B,0</td></tr>
<tr><td>C</td><td>A,0</td><td>B,1</td></tr>
<tr><td>D</td><td>A,0</td><td>B,0</td></tr>
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<td>PO1, PO2, PO3,PO4</td>
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<tr>
<td>13</td>
<td>a)Obtain state diagram for the given state table
b)Reduce the given state table
<table>
<tr><td rowspan="2">PS</td><td colspan="2">NS,Z</td></tr>
<tr><td>X=0</td><td>X=1</td></tr>
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<td>PO1, PO2, PO3,PO4</td>
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<td>14</td>
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<tr><td>X=0</td><td>X=1</td></tr>
<tr><td>A</td><td>B,0</td><td>E,0</td></tr>
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<td>PO1, PO2, PO3,PO4</td>
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</table>

	E	B,0	F,0	Design a clocked sequential circuit for the given state table	
	F	B,0	G,1		
	G	B,0	G,1		
	Using D flip flop				
15	Design a clocked sequential circuit for the given state table Using T flip flop				PO1, PO2, PO3,PO4

PS	NS,Z	
	X=0	X=1
A	A,0	B,0
B	D,0	C,0
C	A,1	B,0
D	B,1	A,1